IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: SERGIO ET AL. Serial No. NOT YET ASSIGNED Filing Date: HEREWITH For: METHOD OF READING A CAPACITIVE SENSOR AND RELATED INTEGRATED CIRCUIT	I HEREBY CERTIFY THIS PAPER OR FEE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED BELOW AND IS ADDRESSED TO: BOX PATENT APPLICATIONS, U.S. PATENT AND TRADEMARK OFFICE, ARLINGTON, VA 22202. EXPRESS MAIL NO: EL 768537397 DATE OF DEPOSIT: November 26, 2001 NAME: DAWN KIMLER SIGNATURE: Dawn Kimler

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for a proposed drawing modification as indicated in red ink to label FIG. 1 as prior art.

In the Claims:

Please cancel Claims 1 to 7.

Please add new Claims 8 to 24.

8. A method of reading a capacitive sensor comprising an array of capacitors ordered in rows and columns functionally connected through row lines and through column lines substantially orthogonal to each

other, using a biasing and reading circuit comprising column and row selectors, and a charge amplifier outputting a voltage of the capacitance of a selected capacitor of the array, the method comprising:

resetting an output voltage of the charge amplifier;

connecting nonselected row and column lines of the array to a reference voltage;

connecting one of an auxiliary capacitor and the selected capacitor to an inverting input of the amplifier while connecting the other one of the auxiliary capacitor and the selected capacitor to define a feedback capacitor of the amplifier; and

applying a step voltage on the capacitor that is connected to the inverting input of the amplifier and reading the output voltage at steady-state.

9. The method of Claim 8, further comprising sequentially scanning the capacitors of the array to obtain a frame of capacitance values of the sensor.

10. The method of Claim 9, wherein the scanning is repeated at a predetermined frame frequency.

11. A method of reading a capacitive sensor comprising an array of capacitors connected in rows and columns, the method comprising:

providing a biasing and reading circuit comprising

column and row selectors,

an amplifier, connected to the column and row selectors, for outputting a voltage of the

capacitance of a selected capacitor of the array, and

an auxiliary capacitor connected to the column and row selectors;

connecting nonselected rows and columns of the array to a reference voltage;

connecting one of the auxiliary capacitor and the selected capacitor as an input of the amplifier while connecting the other one of the auxiliary capacitor and the selected capacitor to define a feedback capacitor of the amplifier; and

applying a step voltage on the capacitor that is connected an the input of the amplifier and reading the output voltage at steady-state.

12. The method of Claim 11, further comprising resetting the output voltage of the charge amplifier.

13. The method of Claim 11, further comprising sequentially scanning the capacitors of the array to obtain a frame of capacitance values of the sensor.

14. The method of Claim 13, wherein the scanning is repeated at a predetermined frame frequency.

15. A system for reading a capacitive sensor comprising an array of capacitors connected in rows and columns, the system comprising:

a biasing and reading circuit comprising an amplifier for outputting a voltage representing the capacitance of a selected capacitor, an auxiliary capacitor, configuration switches for coupling one of the

auxiliary capacitor and the selected capacitor as a feedback capacitor and for coupling the other of the auxiliary capacitor and the selected capacitor to an input of the amplifier, and an analog-to-digital converter for converting the output voltage to digital data;

an input interface circuit for connecting deselected row lines and column lines of the array to a reference voltage and for coupling the selected capacitor of the capacitive sensor to the biasing and reading circuit;

a microprocessor for performing noise filtering and real-time correction of data; and

a digital output interface circuit controlled by the microprocessor for outputting the digital data representing read values of capacitance of the sensor.

16. The system according to Claim 15, wherein the input interface circuit comprises row and column selectors; and further comprising a timing signal generator, controlled by the microprocessor, for generating timing signals for the row and column selectors, for the biasing and reading circuit and for the converter, for synchronizing the operation phases of the circuits.

17. The system of Claim 16, wherein the waveform generator comprises:

a shift register for cyclically producing the timing signals with a certain frequency; and

a finite states machine, controlled by the microprocessor unit, for configuring the shift register.

18. The system according to Claim 15, wherein the input interface circuit comprises:

a selection logic circuit controlled by the microprocessor unit for producing selection signals; and

a plurality of connection modules for connecting the deselected rows and columns to the reference voltage, and for coupling the selected capacitor to the biasing and reading circuit based upon the selection signals.

19. An integrated circuit for reading a capacitive sensor comprising an array of capacitors connected in rows and columns, the circuit comprising:

column and row selectors;

an amplifier, connected to the column and row selectors, for outputting a voltage of the capacitance of a selected capacitor of the array;

an auxiliary capacitor connected to the column and row selectors;

configuration switches for coupling one of the auxiliary capacitor and the selected capacitor as a feedback capacitor and for coupling the other of the auxiliary capacitor and the selected capacitor to an input of the amplifier; and

a controller for controlling the configuration switches.

20. The circuit according to Claim 19, further comprising:

an analog-to-digital converter for converting the output voltage to digital data; and

a digital output interface circuit for outputting the digital data representing read values of capacitance of the sensor.

21. The circuit according to Claim 19, wherein the controller comprises a timing signal generator for generating timing signals for the row and column selectors.

22. A capacitive sensor device comprising:

an array of capacitors connected in rows and columns; and

a reading circuit for reading the array of capacitors and comprising

column and row selectors,

an amplifier, connected to the column and row selectors, for outputting a voltage of the capacitance of a selected capacitor of the array,

an auxiliary capacitor connected to the column and row selectors,

configuration switches for coupling one of the auxiliary capacitor and the selected capacitor as a feedback capacitor and for coupling the other of the auxiliary capacitor and the selected capacitor to an input of the amplifier, and

a controller for controlling the configuration switches.

23. The device according to Claim 22, wherein the reading circuit further comprises:

an analog-to-digital converter for converting the output voltage to digital data; and

a digital output interface circuit for outputting the digital data representing read values of capacitance of the sensor.

24. The device according to Claim 22, wherein the controller comprises a timing signal generator for generating timing signals for the row and column selectors.

REMARKS

For better readability and the Examiner's convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability. It is believed that all of the claims are patentable over the prior art. Accordingly, after the Examiner completes a thorough examination, a Notice of Allowance is respectfully requested in due course. If any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

PAUL J. DITMYER
Reg. No. 40,455
Allen, Dyer, Doppelt, Milbrath & Gilchrist, P.A.
255 S. Orange Avenue, Suite 1401
Post Office Box 3791
Orlando, Florida 32802
407-841-2330
407-841-2343 fax
Attorneys for Applicants